Supplementary Information on Program Control Instructions

Supplement to table 10-7, page 527 in Mano & Kime 4th edition.

Name	Mnemonic	RTL description	Example	Comments on the example
Branch	BR n	PC ← PC + n	BR 05h	; skips 5 addresses of instructions
			BR FBh	; skips back 5 address of instructions (or ; skips –5 addresses. The FBh is 2C for ; –5 base 10)
Jump	JMP nn (or JP)	PC ← nn	JMP 1900h	; skips to address 1900h
Call	CALL nn	(SP) ← PC SP ← SP – 1 PC ← nn	CALL 1900h	; saves return address on stack, ; decrements stack pointer, then ; skips to address 1900h
Return	RET	SP ← SP + 1 PC ← (SP)	RET	; increment the stack pointer, then ; skip back to the return address that was ; previously saved on the stack.
Compare	CMP r (or CP)	ACC – r	CP B	; subtract contents of register B from the ; accumulator and set flag bits according ; to the result. Does not save the result ; anywhere. (Only affects the flag bits).
Test	TEST r r'	r ^ r'	TEST 0900h, B	; bitwise AND of the data word 0900h ; and data stored in register B. Sets the ; flag bits according to the result. Does
	or	or		; not save the result anywhere. (Only ; affects the flag bits.)
	TEST r	ACC ^ r	TEST B	; uses implied addressing to do a bitwise ; AND of the accumulator and the data ; stored in register B. Otherwise the ; same as above.

Note: n denotes relative addressing mode (an 8-bit two's complement number in these examples).
nn denotes direct addressing mode (a 16-bit unsigned binary number in these examples.)
r denotes any operand, typically using register or immediate mode addressing
r' denotes the same as "r" only a different operand