Dordt College, Engineering Department
EGR 323, Electronics II
Spring 2015

2014–2015 Catalog Description	**EGR 323 Electronics II (4 credit hours)** (Spring, Odd) A continuation of Engineering 322. Topics include biasing strategies for discrete and integrated circuit designs, current mirrors, differential and multistage amplifiers, frequency response, feedback and stability. The laboratory includes construction of a kit, which introduces students to power output stages, tuned amplifiers, and demodulator circuits. The laboratory also includes a short design problem. Prerequisite: Engineering 322.
Textbook	Sedra and Smith, *Microelectronic Circuits*, 6th ed., Oxford, 2010. (ISBN 978-0-19-532303-0)
References	Horowitz and Hill, *The Art of Electronics*, 3rd ed., Cambridge University Press. Tuinenga, Paul W., *SPICE: A Guide to Circuit Analysis and Simulation Using Pspice*, 3rd edition, Prentice Hall, 1995.
Instructor	Douglas F. De Boer, Professor of Engineering, http://homepages.dordt.edu/ddeboer Office Phone: 712-722-6245; Office location: SB237 (Office hours posted on homepage, or just call.) E-mail Douglas.DeBoer@Dordt.edu, Home Phone: 722-1414, please call before 10 PM.
Goals	*Creational Structure*: Students will understand elementary semiconductor device physics at the level of equations which model the terminal characteristics of diodes and transistors. This means that students will be able to represent a diode or transistor circuit via a well labeled schematic drawing, derive appropriate equations from the schematic, and know how to solve those equations. Students will be able to carry out these analyses in the frequency domain when appropriate. *Creational Development*: Students will be able to apply several design techniques for stabilizing bias levels. They will understand tradeoffs involved in choosing a bias technique. Students will be able to design circuits involving one or two transistors used in well-known configurations such as a current mirror, cascode amplifier, feedback amplifier, etc. They will understand a historical perspective of how these techniques have improved over time. This will be the main goal of this course.
Prerequisites by topic	Calculus, Linear Systems, A first course in electronics covering diodes, rectifier, clamping and clipping circuits and FET transistors used in logic gates and single-stage amplifiers..
Lecture Topics	BJT Transistors and applications (8 classes) IC design philosophy and multi-transistor circuits including differential amplifiers (12 classes) Frequency response (7 classes) Feedback (9 classes) Stability (3 classes) Tests and review (5 classes) (Three 50 minute lectures per week, MWF)
Lab Topics	One design project running concurrently with the construction of an AM/FM radio (7 week) BJT applications (3 weeks) Single transistor BJT circuits (2 weeks) Miscellaneous topics including current mirrors, network analyzer, CMOS and TTL gates (4 weeks) (One Three-hour lab session per week
Computer Use	Orcad-Pspice is used for circuit simulation. Students are encouraged (but not required) to use programs such as Mathcad or Matlab for homework solutions when appropriate.
Academic Integrity	Students must do their own work and on time. Students may discuss homework but may not show papers to each other. Detail on this policy can be found on the web at http://homepages.dordt.edu/ddeboer/S15/HWSTDS15.HTM#DYOW. See the section headed "Do Your Own Work." This policy applies to the whole course, not just homework.
Accommodations	Students who require assistance or accommodations based on the impact of a documented disability must contact Marliss Van Der Zwaag, the Coordinator of Services for Students with Disabilities to access accommodations. Telephone 722-6490, e-mail Marliss.VanDerZwaag@dordt.edu
Means of Evaluation	Homework (10%), Two Tests (25% each), Final Exam (25%), Lab (15%). For details, follow the link titled "grading policy" at http://homepages.dordt.edu/ddeboer

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Class Dates			Class (8:00 – 8:50 p.m. MWF)	Laboratory (2 PM Mon..)
	1/14	1/16	BJT's: Device structures and terminal characteristics *Text: Chapter 6*	No lab
1/19	1/21	1/24	BJT's: Bias techniques and small signals *Text: Chapter 6*	1.) Logic Gates
1/26	1/28	1/30	BJT's: The three BJT amplifier configurations *Text: Chapter 6*	2.) Class B and Class C Amplifiers
2/2	2/4	2/6	IC design philosophy& Cascode amplifiers *Text: Chapter 7*	3.) Design Project
2/9	2/11 No class on 2/13, reading day		Current mirrors & Darlington and Sziklai transistor pairs *Text: Chapter 7 and pages 952, 953 of Chapter 11*	4.) AM/FM Radio Project, AF Section (Design Project continues)
2/16	2/18	2/20	Differential amplifiers *Text: Chapter 8*	5.) AM/FM Radio Project, AM detector, IF, and mixer sections
2/23	**2/25**	2/27	Non-ideal characteristics of differential amplifiers, *Text: Chapter 8* **Test #1 Wednesday 2/25**	6.) AM/FM Radio Project, AM RF section and alignment.
3/2 (Spring Break, 3/7 – 3/16)	3/4	3/6	Frequency Response *Text: Chapter 9*	7.) AM/FM Radio Project FM detector and IF and mixer sections
	3/18	3/20	Frequency Response *Text: Chapter 9*	(No lab, Spring Break)
3/23	3/25	3/27	Frequency Response *Text Chapter 9*	8.) AM/FM Radio Project FM RF section and alignment.
3/30	4/1	4/3	Feedback: Four configurations *Text Chapter 10*	9.) Conclusion of the design project
4/6	4/8	**4/10**	Feedback: Stability *Text Chapter 10* **Test #2, Friday, 4/10**	10.) Multi-Transistor Circuits
4/13	4/15	4/17	Feedback: Compensation *Text: Chapter 10*	11.) Introduction to the network analyzer
4/20	4/22	4/24	Output stages *Text: Chapter* 11	To Be Announced
4/27	4/29	5/1	Review and catch up	(no lab—dead week)
Thursday, **5/7**			**Final Exam 10:30 am – 12:30 p.m**.	

The above class and laboratory schedules may vary by up to two weeks to accommodate the interests and abilities of the students in this semester's class. A corresponding amount of content may be added to or deleted from the syllabus as needed.