DORDT COLLEGE
ENGINEERING DEPT. **NAME**
COURSE EGR 204 **SUBJECT** **PAGE** **OF** **DATE**

7–A The type ‘175 TTL chip (Also known as a quad D-type flip-flop) is similar to the register shown in your text on page 337 in Figure 1. The main differences are that the '175 has both positive- and negative-true outputs available whereas the register shown in Figure 7-1 has only positive true outputs. A datasheet for the ’175 is available on the course's homework page. A model of the '175 is available in Altera’s Maxplus2 library as part of the Quartus II software program.

Using either manual or computer-based simulation, develop a set of waveforms for the input and output signals for the type ’175 4-bit register. The set of waveforms should illustrate on five successive clock cycles the following actions:

Clear
Load with the number –3 (negative three)
Load with the number +5 (plus five)
Load with the number –1 (negative one)
Clear.

Use two’s complement number formats. Be sure to specify the significance of each bit.
(State: “Signal Q_0 is least significant” or “Signal *A* is least significant” or equivalent, depending on how you label your signals.)

Hint: The D-input signal must be stable during setup and hold times. Even in a “functional” simulation where the setup and hold times are minimal (ε, as ε approaches zero), they are not presumed to be exactly zero. For details, review Section 6-3 on “Flip-Flop Timing” which starts on page 306 of your text. One way to work with this in a vector waveform file is to make your clock signal take, say for example, 10 grid units per clock cycle (five grid units high, five grid units low) instead of two grid units per clock cycle (one high, one low).