Dordt College, Engineering Department

EGR 204, Introduction to Microprocessors and Digital Circuits

Spring 2013

2012–13 Catalog Description

Digital circuits are covered, from simple logic gates through elementary microprocessor architecture. The course begins with elementary logic for binary systems, Boolean algebra, binary integer number formats and arithmetic and combinational design. Intermediate topics include synchronous state machine design and register level concepts. The course concludes with topics in microprocessor architecture that include elementary assembly language and interfacing. Laboratory provides hands-on experience in logic design and microprocessor interfacing and includes two formal design projects. This course serves both computer science and engineering students. Prerequisite: Physics 116 or Physics 202 or Engineering 103. (4 credit hours)

Textbook

M. Morris. Mano and Charles R Kime, *Logic and Computer Design Fundamentals*, 4th edition, Prentice-Hall, 2008. ISBN 0-13-198926-X

References

Hayes, *Introduction to Digital Logic Design*, Addison Wesley
Bartee, Thomas C., *Digital Computer Fundamentals*, McGraw-Hill.

Instructor

Douglas F. De Boer, Professor of Engineering, http://homepages.dordt.edu/~ddeboer
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Course Objectives and Outcomes

Creational Structure: Students will understand the laws of logic needed for designing digital circuits.

Creational Development: Students will be able to use basic laboratory equipment such as power supplies, logic probes, and logic simulators as tools for analysis. They will design and demonstrate combinational and sequential circuits with limited numbers (about 4) of inputs, outputs and state variables. They will test circuits that interface to a microprocessor. They will be able to use a microprocessor trainer to test simple machine code and prototype circuits.

Prerequisites by topic

Introductory DC circuits as presented in typical high-school physics classes, high-school algebra, and freshman college level problem solving skills in a science or engineering context.

Lecture Topics

Logic Gates, Boolean Algebra, Karnaugh Maps	(7 classes)
Combinational logic design techniques	(8 classes)
Binary integer number systems, codes, arithmetic	(4 classes)
Flip-Flops and Sequential logic	(4 classes)
Registers and Register Transfer Operations	(2 classes)
Memory and Programmable Logic	(3 classes)
Data Path and Control Logic Design for a CPU	(4 classes)
Microprocessor and/or Microcontroller	(5 classes)
Tests and review	(5 classes)

(Three 50 minute classes per week, MWF at 8 AM in room SB216)

Lab Topics

TTL Circuits and use of equipment	(1 week)
Logic Simplification, hierarchy, VHDL	(2 weeks)
Combination Logic Design Project & Programmable logic	(3 weeks)
Binary Arithmetic and MSI Logic Functions	(1 week)
Flip-Flops and Synchronous Sequential Logic	(4 weeks)
Microprocessor trainer experience	(2 weeks)

(One Three-hour lab session per week, Thursdays at 2–5 PM in room SB233, the EE lab.)

Computer Use

A logic simulator and programmer is introduced (Altera's Quartus II),
Students write and run short machine language programs. Assembly of code is done by hand.

courses@dordt

Most assignments and handouts are available via Dordt's course management system, "courses@dordt." The logon URL is http://courses.dordt.edu. Use your Dordt College network user ID and password. Then drill down to the EGR 204 course.

Academic Integrity

Students must do their own work. Students may discuss homework but may not show papers to each other outside of peer grading. Detail on this policy can be found on the web at http://homepages.dordt.edu/~ddeboer/S13/HWSTDS13.HTM#DYOW. See the section headed "Do Your Own Work." This policy applies to the whole course, not just homework.

Accommodations

Students who require assistance or accommodations based on the impact of a disability must contact the Coordinator of Services for Students with Disabilities, Marliss Van Der Zwaag, to access accommodations. Telephone 722-6490, e-mail Marliss.VanDerZwaag@dordt.edu

Means of Evaluation:

Homework (10%), Two Tests (24% each), Final Exam (27%), Lab (Two reports, ~7.5% each).
For details, follow the "grading philosophy" link at http://homepages.dordt.edu/~ddeboer

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Class meets for three 50-minute periods per week, Mon., Wed., and Fri., 8:00 – 8:50 AM in Room SB216
Lab meets for one 3-hour meeting per week, Thursday in Room SB233, 2:00 to 5:00 PM

Dates			Class	Laboratory
	1/16	1/18	Introduction, Binary Numbers and Codes Text Chapter 1, Sections 1-1, 1-2, 1-5	No lab this week (First week of class)
1/21	1/23	1/25	Logic Gates, Boolean Algebra Text: Chapter 2, Sections 2-1 thru 2-3	1.) Safety and Introduction. to the Equipment
1/28	1/30	2/1	Karnaugh Maps, Sufficient Sets of Gates Text: Chapter 2, Sections 2-4 to the end	2.) DeMorgan's Theorems and Logic Simplification
2/4	2/6 No class on Friday Reading Day		Combinational logic, HDL & Simulation Text: Chapter 3, Sections 3-1 thru 3-6.	3.) Introduction to hierarchical design and VHDL
2/11	2/13	2/15	Combinational Functions—Nonarithmetic Text, Chapter 3., Sections 3-7 thru 3-8 **Test #1 Wednesday, 2/13**	4.) Combinational Logic Design Project & Programmable Logic (1st of 3 weeks)
2/18	2/20	2/22	Combinational Functions—Nonarithmetic Text: Chapter 3, Section 3-9 to the end	5.) VHDL and also Design Project (2nd wk)
2/25	2/27	3/1	Combinational Functions—Arithmetic Text: Ch. 1 Sec 1-3, 1-4 and Ch 4	Design Project (3rd wk)
3/4	3/6	3/8	Latches and Flip-Flops Text: Chapter 5, Sections 5-1 thru 5-3	6.) Binary Arithmetic and MSI Combinational Logic Functions
(Spring Break is 3/16–3/18)				
	3/20 No class on Monday, 3/18, Spring Break	3/22	State Machines Text: Chapter 5, Secs. 5-4, 5-5, 5-7, 5-10.	7.) Introduction to Flip-Flops
3/25	3/27	3/29	Registers Text: Chapter 7 omit Sections 7-11, 7-12, 7.13 **Test #2 Wednesday, 3/27**	8.) Synchronous State Machine Design (1st of 3 weeks)
4/1	4/3	4/5	Memory and Programmable Logic Text Chapter 8	No Lab this week (Assessment Day)
4/8	4/10	4/12	CPU and Microprocessor Basics Text Chapter 9	Design Project (2nd wk)
4/15	4/17	4/19	Assembly Language Text Chapter 10	Design Project (3rd wk)
4/22	4/24	4/26	I/O and Communication Text Chapter 12	9) Introduction to a Microprocessor
4/29	5/1	5/3	Review or catch-up	10.) Writing and Assembling a Program
Week of Exams 5/7			**Final Exam** **Tuesday, 5/7 3:30 – 5:30 p.m.**	

The class and laboratory schedules may vary by up to two weeks to accommodate the pace of this particular group of students.
This could require the deletion or addition of a corresponding amount of course content.