PROBLEMS ON DIGITAL SIGNALS SENT VIA TRANSMISSION LINES

2.1 Assume that a very long lossless transmission line has a short stub attached in parallel near the middle of the line, and that the stub is terminated with an infinite impedance. The stub is made from the same type of transmission line as the main line. At some time in the distant past, t_{past} a switch at the source end of the transmission line caused a 1 V step wave to start traveling down the transmission line. Eventually the 1 V step wave arrives at the tap. Assume that it takes 10 ns for a signal to travel from the tap to the open end of the stub. Of course, then it takes another 10 ns for a reflection to travel from the open end of the stub back to the tap. Assume that the transmission line has an initial condition prior to t_{past} of 0 V and 0 A everywhere along the line and the stub. Let the reference time of $t = 0$ be the time when an incident signal caused by the action of the switch first reaches the tap. Time t_{past} will be such a large magnitude negative value that for the sake of this problem's timeframe of interest, any waves launched into the transmission line from the tap never reach the source or the load ends of the main transmission line.

Calculate the voltage at the tap as a function of time, $v_T(t)$ where the stub leaves the line, and at the open end of the stub, $v_X(t)$ in response to a step voltage (from 0 to 1 V) impressed at one end of the line.

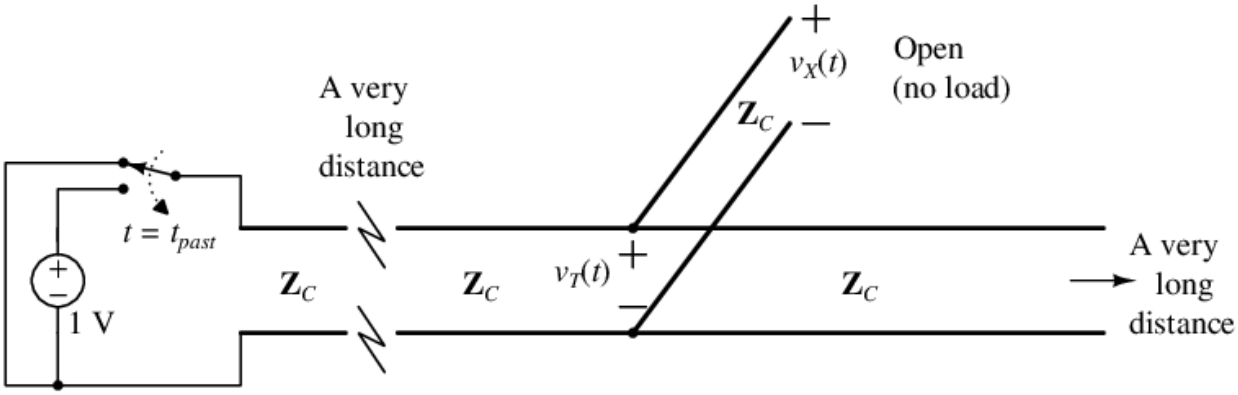

Figure P2.1, The transmission line described in Problem 2.1.

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2.2 You are given a pair of devices with a transmission line running between them, and you are to **determine the maximum rate of transmission of signals (in bits per second) between the devices under various termination conditions**.

A digital gate at the receiving end of the transmission line must have a signal present for 10 ns at a voltage of 0.8 V or less for the entire 10 ns for a logic-0 to be reliably detected. This same gate must have a signal present for 10 ns at a voltage of 2 V or more for the entire 10 ns for a logic-1 to be reliably detected. This same gate has an input impedance of Z_L (entirely real—resistive only).

The digital gate at the sending end of the transmission line has an open-circuit Thevenin equivalent voltage of 0.3 V if it is sending logic-0 and 3.3 V if it is sending logic-1. This gate has a Thevenin equivalent output impedance of Z_S (entirely real—resistive only).

The transmission line has a length of 9 feet. The characteristic impedance of the transmission line is $Z_0 = 50\ \Omega$ (entirely real—resistive only) It takes 10 ns for a signal to propagate from one end to the other. ($V_P = 0.9c$ where c is the speed of light) The transmission line is lossless.

What is the maximum rate of transmission in bits/second if. . .

a.) $Z_S = 0$ and $Z_L = Z_o$ (The load is matched to the transmission line.)

b.) $Z_S = Z_0$ and $Z_L = \infty$ (The source is matched to the transmission line, the load is high-*Z*.)

c.) $Z_S = 3Z_0$ and $Z_L = 9Z_0$

d.) $Z_S = 9Z_0$ and $Z_L = 3Z_0$

e.) Assume an additional logic gate having the same voltage and timing characteristics as described above and having an infinite input impedance and connected via a very short stub (practically zero length) can be tapped at any arbitrary position along the transmission line. Assuming conditions of part (a) above, what is the maximum rate of signaling for valid logic from both the gate at the load end of the line and the gate at the tap?